



APPENDIX

Please amend claim 1 as follows:

1. (Amended) A method comprising:
forming a metal oxide semiconductor radio frequency circuit element over a triple well in a substrate; and
biasing a well of said triple well through a resistor.

Please cancel claim 6 without prejudice.

Please amend claim 20 as follows:

20. (Amended) A method comprising:
forming a first metal oxide semiconductor radio frequency circuit element over a triple well in a substrate;
biasing a first well of said triple well through a first resistor with a first bias potential;
forming a second metal oxide semiconductor radio frequency circuit element over a second triple well in a substrate; and
biasing a second well of said second triple well through a second resistor coupled to said first bias potential.

Please cancel claim 25.

Please amend claim 26 as follows:

26. (Amended) The method of claim [25] 20 including biasing said wells through resistors having a resistance greater than 100 ohms.

Please add the following new claims 30 *et seq.*:

31. (New) A method comprising:
forming a metal oxide semiconductor circuit element over a triple well in a substrate;
operating said circuit element at a radio frequency; and
biasing a well of said triple well through a resistor which acts as a high impedance relative to a junction capacitance within the triple well.

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In view of the remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,

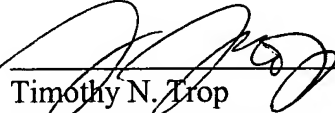
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PATENT TRADEMARK OFFICE

A handwritten signature in dark ink, appearing to read "Timothy N. Trop", written over a horizontal line.

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32. (New) The method of claim 31 including forming an integrated inductor over said triple well.

33. (New) The method of claim 31 including forming a P-type well in an N-well formed in said substrate.

34. (New) The method of claim 33 including biasing the N-type and P-type wells through different resistors.

35. (New) A method of claim 31 including providing a common bias potential to different wells through separate resistors for each well.

36. (New) The method of claim 35 including biasing said wells through resistors having a resistance greater than 100 ohms.

37. (New) The method of claim 31 including coupling a resistor to an N-well within said triple well on a P-type substrate so that said resistor acts as a high impedance relative to the junction capacitance of the N-well to the P-well of the triple well.